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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/395,297	09/13/1999	SOPHIE WILSON	1073/OG116	5799

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EXAMINER
DECKTER, STEPHANIE M

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/395,297	WILSON, SOPHIE	
	Examiner	Art Unit	
	Stephanie M. Deckter	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Preliminary Amendment A as received on 12/08/99; Priority Papers as received on 09/13/99; Formal Drawings as received on 06/09/00; Information Disclosure Statement as received on 06/30/00.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The abstract of the disclosure is objected to because it is more than one paragraph. Correction is required. See MPEP § 608.01(b). Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The attempt to incorporate subject matter into this application by reference to "copending Application No. (PWF Ref: 92472)" in the first paragraph of page 5 is improper because Examiner cannot reference applications without U.S. serial numbers. Please provide the U.S. serial number that corresponds to the copending application PWF Ref: 92472. Appropriate correction is required.

6. The disclosure is objected to because of the following informalities:

a. Please correct the sentence "The computer system described herein is schematically illustrated in Figure 1 is a schematic diagram of the system" on the bottom of page 3 to correctly read "The computer system described herein, and illustrated in Figure 1, is a schematic diagram of the system."

b. On page 11, in the description of figure 7, the specification states that SIMD lanes b_0, b_2, b_3, and b_4 satisfy the condition Carry Set C, or "0011," as held in the TST field of the instruction. However, it appears that only lane b_2 actually holds the identical condition code "0011" and should therefore be the only lane to satisfy the condition. Please correct the specification to reflect such. Furthermore, Figure 7 should also be corrected to show that the only result of the ADD operation to be loaded into the destination register is in lane b_2. Please see the detailed description of all objections to Figure 7 below.

Appropriate correction is required.

Drawings

7. The drawings are objected to because SRC1 in Figure 6 shows packed objects b_0 to b_1 rather than b_0 to b_7 as discussed in the specification in the second paragraph of page 10. A

proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

8. The drawings are objected to because Figure 7 does not accurately illustrate that which has been set forth in the description of such on page 11 of the specification. The specification states that SIMD lanes b_0, b_2, b_3, and b_4 satisfy the test condition. Figure 7 shows that the result has not been loaded into destination register DST in lanes b_2, b_3, b_4, and b_7, i.e. these lanes have not satisfied the condition. If lanes b_0, b_2, b_3, and b_4 satisfy the test condition, then the figure should show an "x" in lanes b_1, b_5, b_6, and b_7 to denote the result being loaded into the DST for lanes b_0, b_2, b_3, and b_4, but not loaded into the DST for lanes b_1, b_5, b_6, and b_7. However, since it appears that only lane b_2 actually holds the condition code "0011," which is identical to the code held in the TST field of the instruction, lane b_2 should therefore be the only lane to satisfy the condition. Therefore, please correct the drawing to reflect such and show an "x" in all lanes of the DST register, except lane b_2 to denote that b_2 has satisfied the condition and its result will be loaded into the DST register in the appropriate lane. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

9. Applicant is advised that should claim 4 be found allowable, claim 6 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight

difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

10. Claim 1 recites the limitation "lanes of the first and second source operands" in the 7th and 8th lines of the claim. There is insufficient antecedent basis for this limitation in the claim as the only prior mention of "lanes" is that of input store lanes as set forth in the 5th line of the claim.

11. Claim 11 recites the limitation "in respective lanes" in the 4th line of the claim. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 12 recites the limitation "said selected codes" in the 3rd line of the claim. There is insufficient antecedent basis for this limitation in the claim.

13. Claims 1 and 11 are objected to because it is unclear which "lanes," i.e. the source operand lanes or the store input lanes, are being referred to in the 6th, 9th, 11th, and 13th lines of claim 1 and the 4th, 5th, and 9th lines of claim 11. For the purposes of Examiner's prior art search, it has been assumed that the limitation "lanes" in the 6th line of claim 1 refers to the store input lanes and all other occurrences of the limitation "lanes," as mentioned above, refer to the source operand lanes. Appropriate correction is required.

14. Claims 4, 6, and 7 are objected to for the following informalities: The limitation "maximum number of lanes in the first and second source operands," as set forth in the 2nd and 3rd lines of claims 4 and 6 and the 2nd, 4th, and 5th lines of claim 7, is unclear. Please correct this limitation to read either "maximum number of lanes in each of the first and second source operand." Appropriate correction is required.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

16. Claim 11 rejected under 35 U.S.C. 102(e) as being anticipated by Yung, U.S. Patent Number 5,996,066 (herein referred to as Yung). Yung has taught a method of executing instructions on operands containing a plurality of packed objects (Yung column 2, lines 13-15), the method comprising:

a. accessing at least one source operand containing a plurality of packed objects in respective lanes (column 8, lines 27-28 and figure 13, element 108);

b. accessing stored condition values to determine for each lane whether or not an operation defined in the instruction is to be implemented on that lane of the operand (column 8, lines 23-30 and column 2, lines 20-22); and

c. carrying out the operation and updating a destination operand only in those lanes for which the stored condition value indicates that the operation should be implemented (column 8, lines 29-37).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1 and 8 (when claim 8 depends from claim 1) are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,996,066 (herein referred to as Yung). Referring to claim 1, Yung has taught an execution unit for use in a computer system for conditionally carrying out an operation defined in a computer instruction, the execution unit comprising:

a. first input store (Yung figure 9A and 13, element 108) for holding a respective first operand on which an operation defined in the instruction is to be carried out (Yung column 8, lines 29-30 and figure 13, element 116), wherein each store defines a plurality of lanes each holding an object (Yung column 7, line 59 to column 8, line 4);

b. a plurality of operators associated respectively with the lanes for carrying out an operation specified in the instruction on objects in corresponding lanes of the first source operand (Yung column 8, lines 24-27 and figure 13, element 116);

c. a destination buffer for holding the results of the operation on a lane-by-lane basis (Yung column 8, lines 27-28 and 33-35 and figure 13, element 114); and

d. selecting means (Yung column 8, lines 23-30 and figure 13, elements 116 and 114) for determining for each lane in dependence on stored condition values whether or

not the operation is to be executed on objects in that lane (Yung column 7, line 64, column 8, line 23-30 and figure 13, element 112 and column 2, lines 20-22).

Yung has not explicitly taught first and second input stores for holding first and second operands. However, Yung has taught first and second operands for each instruction (Yung column 6, lines 17-35 and figure 6B, elements 68a (please see RS1 and RS2) and 68b (please see RS1 and RS2)). Since Yung has further taught conditionally performing an arithmetic operation on particular fields of a single operand (Yung column 8, lines 23-28), it would logically follow that conditional execution of an arithmetic operation would be performed between particular fields of two operands as provided in the two source registers shown in the instruction formats taught by Yung (Yung column 6, lines 17-35 and figure 6B, elements 68a (please see RS1 and RS2) and 68b (please see RS1 and RS2)). Doing so would then necessitate first and second input stores for holding the first and second operands. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide two input stores for holding first and second operands.

18. Referring to claim 8, when claim 8 depends from claim 1, Yung has taught a computer system for conditionally carrying out an operation defined in a computer instruction, the computer system comprising:

a. fetch and decode circuitry for fetching and decoding a sequence of instructions from a program memory (Yung figure 1, elements 46 and 44a);

b. at least one execution unit **according to claim 1** (Yung figure 1, elements 48, 30, 31, 25, 26, and 28); and

c. at least one memory access unit for effecting memory access operations responsive to memory access instructions (Yung figure 1, elements 48, 44b, and signal "TO/FROM MEMORY").

19. Claims 2-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,996,066 (herein referred to as Yung) in view of Flynn, Computer Architecture Pipelined and Parallel Processor Design, 1995 (herein referred to as Flynn). Referring to claim 2, Yung has taught each limitation of claim 1 from which this claim depends, including predicated execution of the objects in each lane in dependence on stored condition values (Yung column 2, lines 20-22). Yung has not taught stored condition values comprising a set of condition codes. Flynn has described the well-known notion that instructions are conditionally executed based on testing the state of various condition codes (Flynn page 163, Section 3.4.4 Condition Code Testing). Flynn has further discussed that condition codes are a concise way to store results of previously executed instructions, such as positive, negative, zero, or overflow values (Flynn pages 30-31, Section 1.5.4 Branches). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize condition codes as the stored condition values to determine whether or not the operation is to be executed on objects in each lane.

20. Referring to claim 3, Yung has taught selecting means (Yung column 8, lines 23-30 and figure 13, elements 116 and 114) for determining whether or not the operation will be performed on the objects in each lane. Yung has also taught a comparison operation that generates a mask (Yung column 5, lines 45-47 and figure 5, elements 64 and 55c) used by the selecting logic to determine which lane will be operated upon (Yung column 8, lines 23-30 and figure 13, elements

116 and 114). Yung has not taught the selecting means comprising means for comparing selected ones of said set of condition codes with a test code identified in the instruction. As discussed above in the rejection of claim 2, Flynn has taught predicated execution based on the results of testing various condition codes (Flynn page 163, Section 3.4.4 Condition Code Testing), such testing comprising a comparison between the stored condition code values and a particular test code provided by the instruction (Flynn page 30, Table 1.14 See "BC.NE"). Since the mask of Yung utilized to determine which lanes will be operated upon is generated by comparison logic, it would have been obvious to one of ordinary skill in the art at the time the invention was made that such comparison logic must have comprised the traditional comparison between condition codes and the test code provided by the instruction. Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to move the comparison circuitry into the selecting logic of Yung such that the system would have required less time and space to perform the comparison in real time for each lane as opposed to storing the results of the comparison operation in the mask register and then later using that mask to determine whether or not the operation in each lane was to be implemented.

21. Referring to claim 4, Yung has not explicitly taught the number of condition codes, corresponding to the maximum number of lanes in the first and second source operands. However, Yung has taught the number of fields in the mask corresponding to the maximum number of lanes in the source operands (Yung figure 13). Therefore, based on the discussion above for the rejection of claim 3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that when the number of mask fields corresponds to the

maximum number of lanes in the operands, there must also be that many condition codes to create the mask fields upon comparison with the test code.

22. Referring to claim 5, Flynn has taught a condition code generator (the ALU) for generating said set of condition codes responsive to execution of an instruction (Flynn page 30, Section 1.5.4 Branches, first paragraph).

23. Claim 6 is rejected for the same reasons as set forth in the rejection of claim 4 above.

24. Referring to claim 7, Yung has taught the number of condition codes in said set corresponds to the maximum number of lanes in the first and second source operands as discussed in the rejection of claim 4 above. Yung has not explicitly taught generation of the set of condition codes so that when the operands have less than the maximum number of lanes, two or more condition codes are set to the same value so that each individual condition code in the set is generated regardless of the degree of packing of the first and second source operands. However, Yung has taught various degrees of packing of the first and second source operands (Yung column 5, lines 47-67 and figure 6A). In order to ensure that execution of all bits of the larger data words, i.e. 32-bit packed data rather than 16-bit packed data, are either enabled or disabled, it would have been necessary to set adjacent condition codes to the same value. Furthermore, doing so would have prevented the problem of the condition codes causing the most significant portion of the data word being operated upon while the least significant portion is disabled. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to set two or more condition codes to the same value to ensure that all condition codes are generated when less than the maximum number of lanes are used within the source operands.

25. Referring to claim 8, when claim 8 depends from any of claims 2-7, Yung has taught a computer system for conditionally carrying out an operation defined in a computer instruction, the computer system comprising:

a. fetch and decode circuitry for fetching and decoding a sequence of instructions from a program memory (Yung figure 1, elements 46 and 44a);

b. at least one execution unit **according to any of claims 2 to 7** (Yung figure 1, elements 48, 30, 31, 25, 26, and 28); and

c. at least one memory access unit for effecting memory access operations responsive to memory access instructions (Yung figure 1, elements 48, 44b, and signal "TO/FROM MEMORY").

26. Referring to claim 9, neither Yung nor Flynn has explicitly taught a condition code register for holding said condition values in the form of a set of condition codes. However, it would have been necessary to store the condition codes set by a previous instruction prior to comparison with the test code provided by the current instruction to determine whether or not the current instruction will execute. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include a condition code register to hold the condition values in the form of a set of condition codes. Official Notice has been taken.

27. Referring to claim 12, Yung has taught the step of accessing stored condition values, i.e. a mask, to determine if the instruction will be implemented on a particular lane (column 8, lines 23-30). Yung has also taught a comparison operation that generates the mask (Yung column 5, lines 45-47 and figure 5, elements 64 and 55c) used by the selecting logic to determine which lane will be operated upon (Yung column 8, lines 23-30 and figure 13, elements 116 and 114).

Yung has not taught the accessing a set of condition codes and comparing them with a test code identified in the instruction. As discussed above in the rejection of claim 2, Flynn has taught predicated execution based on the results of testing various condition codes (Flynn page 163, Section 3.4.4 Condition Code Testing), such testing comprising a comparison between the stored condition code values and a particular test code provided by the instruction (Flynn page 30, Table 1.14 See "BC.NE"). Since the mask of Yung utilized to determine which lanes will be operated upon is generated by the comparison logic, it follows logically that such comparison logic must have comprised the traditional comparison between condition codes and the test code provided by the instruction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that the step of accessing the stored condition value comprises accessing condition codes and then comparing them with the test code identified in the instruction.

28. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,996,066 (herein referred to as Yung) in view of Flynn, Computer Architecture Pipelined and Parallel Processor Design, 1995 (herein referred to as Flynn) and further in view of Hsu, U.S. Patent Number 5,901,318 (herein referred to as Hsu). Referring to both claims 10 and 13, Flynn has taught predicated execution where a particular test code is provided by the instruction (Flynn page 30, Table 1.14 See "BC.NE"). Neither Yung nor Flynn has taught the test code being held in a test register which is identified by an address in the instruction. Hsu has taught the test code being held in a test register which is identified by an address in the instruction (column 1, lines 45-52). Indirectly addressing the register where the test code is being held allows for the test code to be determined dynamically by the execution of

a previous instruction and stored in the test register identified by the current instruction. This arrangement allows for a more flexible system than identifying the test code as an immediate value. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made for the instruction to identify the address of a test register where the test code was being held.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephanie M. Deckter whose telephone number is 703-308-6132. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Stephanie M. Deckter
Examiner
Art Unit 2183

SMD

February 19, 2002

EDDIE CHAN
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